AND8392/D

A 800 W Bridgeless PFC Stage

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APPLICATION NOTE

Environmental concerns lead to new efficiency requirements when designing modern power supplies. For instance, the 80 plus initiative and moreover its bronze, silver and gold derivatives force desktops and servers manufacturers to work on innovative solutions. An important focus is on the PFC stage that with the EMI filter can be easily consume 5% to 8% of the output power at low line, full load.

Bridgeless PFC is one of the options to meet these new requirements. The main goal of this paper is to present a bridgeless solution that is relatively easy to implement in the sense that it does not require any specific controller and the operation remains very similar to that of a conventional PFC. The solution is illustrated by a 800 W, wide mains application driven by the NCP1653.

Why remove the bridge?

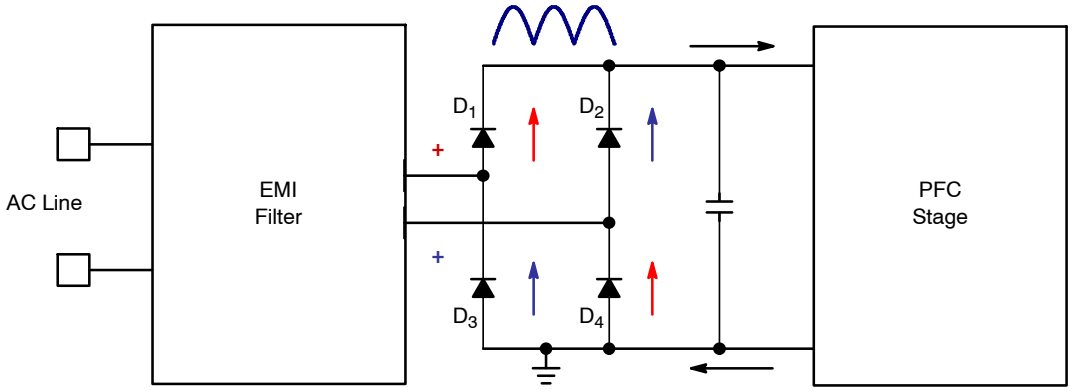

Figure 1. The Input Current Flows Through Two Diodes

Figure 1 portrays the diodes bridge that is usually inserted between the EMI filter and the PFC stage. This bridge rectifies the line voltage to feed the PFC stage with a rectified sinusoid input voltage. It is well known that as a result of this structure, the input current must flow through two diodes before being processed by the PFC boost:

- For one line half−wave, D_1 and D_4 conduct (red arrows of Figure 1)
- For the other one, *D_2 and D_3* convey the current (blue arrows of Figure 1)

As a matter of fact, two diodes of the bridge are permanently inserted in the current path. Unfortunately, these components exhibit a forward voltage that leads to conduction losses.

The mean value of the current seen by the bridge is the line average current. Hence we can write the following equation:

$$\left\langle I_{bridge} \right\rangle_{T_{line}} = \left\langle I_{line}(t) \right\rangle_{T_{line}} = \frac{2\sqrt{2}}{\pi} \cdot I_{line(rms)} \qquad \text{(eq. 1)}$$

The line rms current can be easily expressed as a function of the power and of the line voltage:

$$I_{line(rms)} = \frac{P_{out}}{\eta \cdot V_{in(rms)}} \qquad \text{(eq. 2)}$$

Where:

- P_{out} is the output power
- η is the efficiency
- $V_{in(rms)}$ is the rms line voltage

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Since two diodes permanently see the average line current, the bridge consumes a power that can be computed as follows:

$$P_{bridge} = 2 \cdot V_f \cdot \left\langle I_{bridge} \right\rangle_{T_{line}} \cong 2 \cdot V_f \cdot \frac{2\sqrt{2} \cdot P_{out}}{\eta \cdot \pi \cdot V_{in(rms)}} \quad \text{(eq. 3)}$$

Finally, if we assume a 1 V forward voltage per diode and computing the losses at the usual low line rms voltage (90 V), it comes:

$$P_{bridge} \cong 2 \cdot 1 \cdot \frac{2\sqrt{2} \cdot P_{out}}{\eta \cdot \pi \cdot 90} \cong 2\% \cdot \frac{P_{out}}{\eta} \quad \text{(eq. 4)}$$

"Basic" Bridgeless Architecture

In other words, an input bridge consumes about 2% of the input power at low line of a wide mains application. Hence, if one of the series diodes could be suppressed, 1% of the input power could be saved and the efficiency could for instance, rise from 94% to 95%. Also, the major hot spot produced by a traditional diodes bridge would be eliminated at the benefit of an improved reliability of the application. Here are the motivations behind the bridgeless approach.

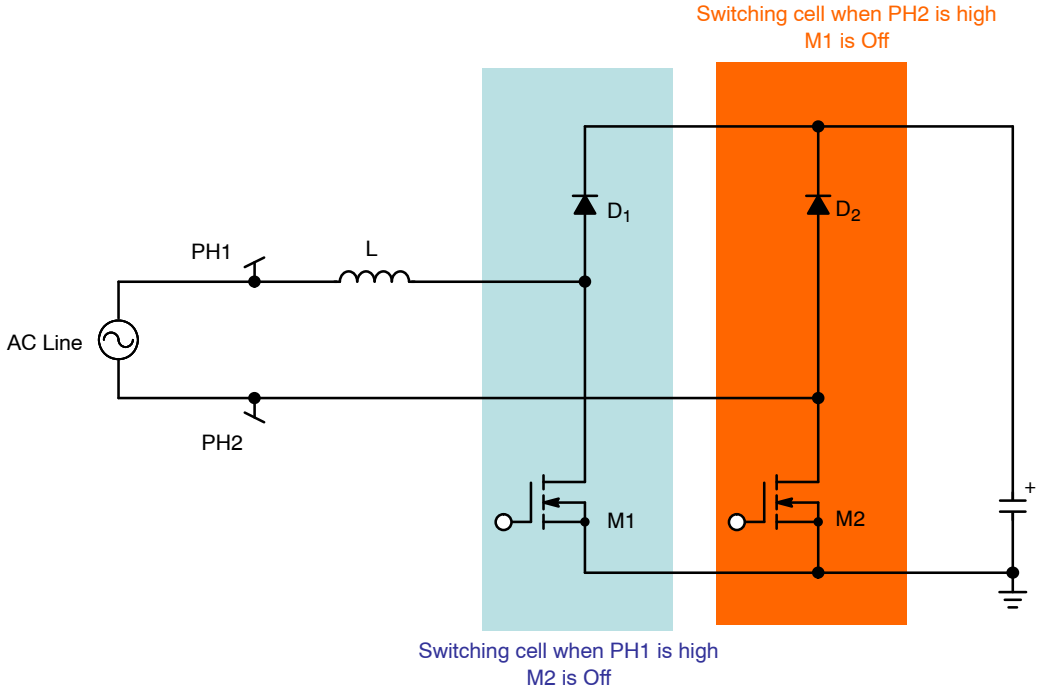

Figure 2. "Traditional" Bridgeless Solution

Figure 2 portrays a classical option for bridgeless PFC. They are two switching cells. Each of them consists of a power MOSFET and of a diode:

- The first cell (M_1, D_1) processes the power for the half−line cycle when the terminal "PH1" of the line is high and is in idle mode for the rest of the line period.
- The second cell (M_2, D_2) is active for the other half−wave when "PH1" is low compared to terminal "PH2".

The line (Note 1) and the PFC inductor are placed in series and the arrangement they form is connected to the switching nodes of the two switching cells.

Figures 3 and 4 show the functioning of the bridgeless PFC when the "PH1" is high. Figure 5 summarizes the operation for the other half−line cycle.

1. The EMI filter that is to be placed in parallel to the line source is not represented for the sake of simplicity.

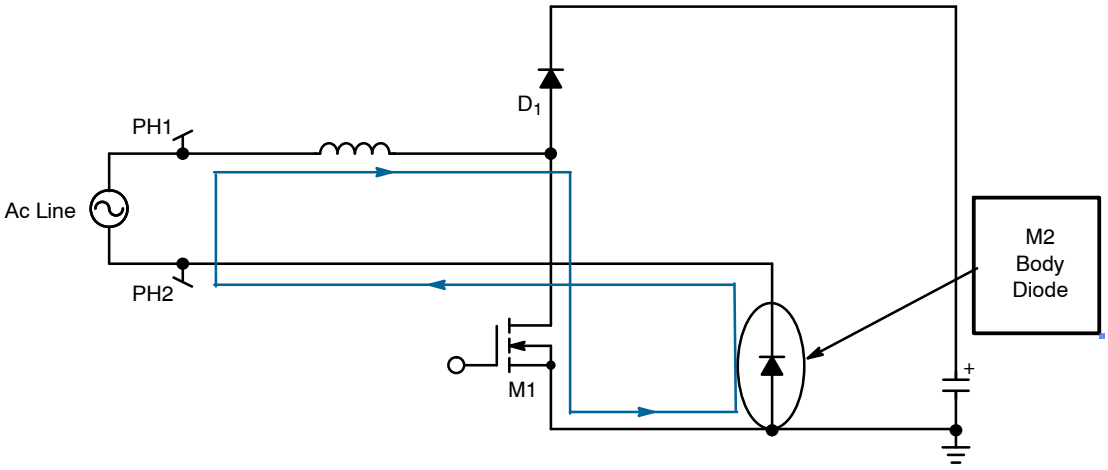

Figure 3. MOSFET Conduction Phase (”PH1” Half−Wave)

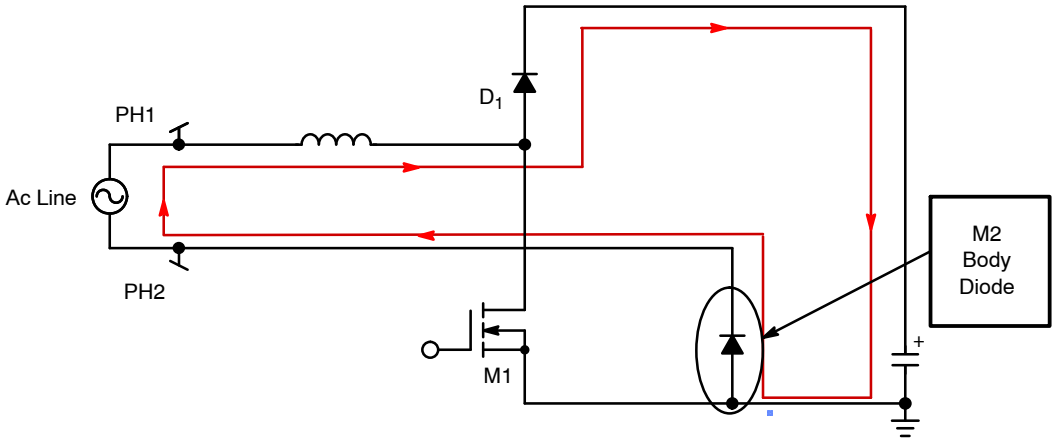

Figure 4. Current Path When the MOSFET is Open (”PH1” Half−Wave)

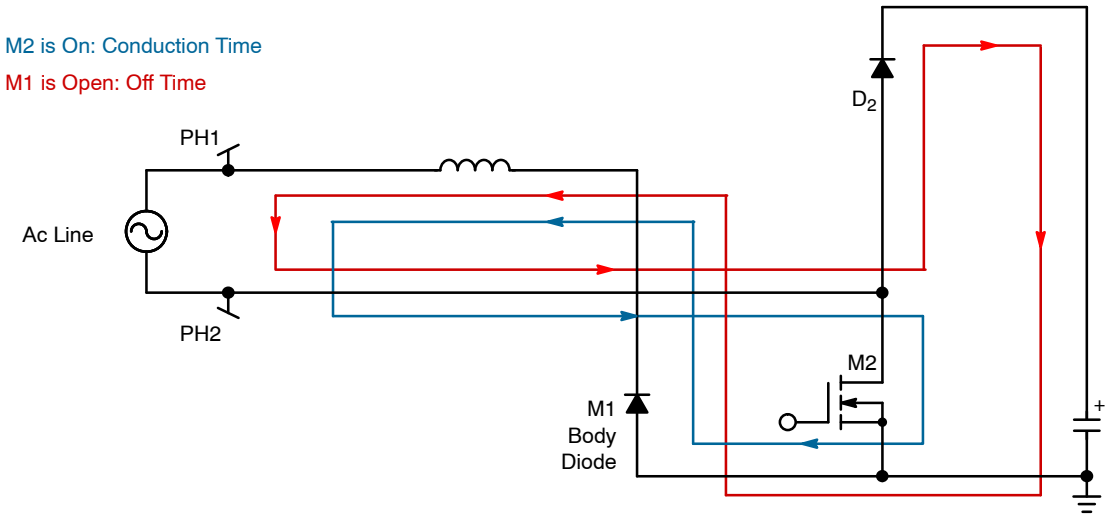

Figure 5. Operation for the Line Half−Wave when ”PH2” is High

As sketched by Figures 3 to 5, the input current is processed by the switching cell that is active for the considered line half−wave. The MOSFET of the inactive cell has a role anyway, since its body diode serves as the current return path.

Compared to a conventional PFC stage, the losses due to the bridge are saved but the body diode of the inactive MOSFET conveys the coil current. Finally, this structure eliminates the voltage drop of one diode in the line−current path for an improved efficiency.

However, the presented architecture presents several inconveniences that actually, result from the fact that the line is not referenced to the ground as it is the case in a conventional PFC. Instead, in this structure, the line is floating compared to the PFC stage ground, leading to the following difficulties:

- Certain PFC controllers need to sense the input voltage. In this structure, a simple circuitry cannot do the job.
- Similarly, the coil current cannot be easily monitored.

Besides these difficulties in the circuit implementation, EMI filtering is the main issue. When ”PH1” is high, the negative terminal ”PH2” is attached to ground by the M_2 body diode. Hence, the application ground is connected to ac line as it happens in a conventional PFC. Now, when ”PH2” is high, the MOSFET M_2 switches and the voltage between the line terminals and the application ground pulses as well. More specifically, the potential of the ”PH2” node nearly oscillates between 0 (when the MOSFET on) and the PFC output voltage (when the MOSFET is off). This large ”dV/dt” leads to an increased common−mode noise that is difficult to filter. This is probably the major drawback of the solution ([1] and [2]).

An improvement consists in splitting the inductor into two smaller ones and to insert one of them between one line terminal and the switching node of cell 1 and the other one between the second line terminal and the switching node of cell 2. Doing so, the large aforementioned ”dV/dt” is no more directly applied to the input terminals and thus, the line potentials can be more stable with respect to the board ground. However, such a solution still exhibits a worse signature in the high frequency part of the spectrum.

2−Phase Approach

Figure 6 portrays another option for bridgeless PFC. This solution was proposed by Professors Alexandre Ferrari de Souza and Ivo Barbi ([3]). As shown by Figure 6, there is no full bridge. Instead, the ground of the PFC circuit is linked to the line by diodes D_1 and D_2 and each terminal feeds a PFC stage. Hence, the solution could be viewed as 2−phase PFC where the two branches operate in parallel:

- For the half−wave when the terminal ”PH1” of the line is high, diode D_1 is off and D_2 connects the PFC ground to the negative line terminal (”PH2”). D_2 grounds the input of the ”PH2 PFC stage” branch that thus, is inactive and the ”PH1 PFC stage” processes the power.
- For the second half−line cycle (when ”PH2” is high), the ”PH2 PFC stage” branch is operating and ”PH1 PFC stage” that has no input voltage, is inactive.

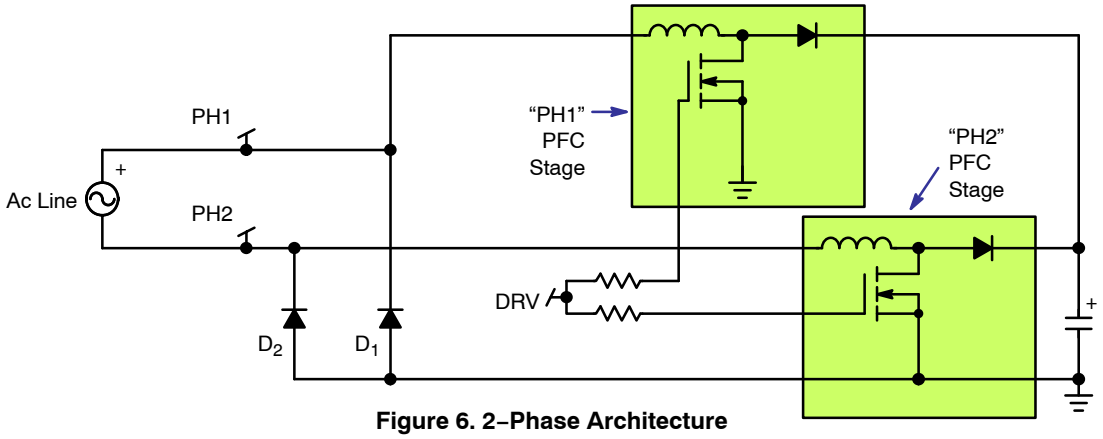

Figure 6. 2−Phase Architecture

Figure 7 gives an equivalent schematic for the two half−waves.

Similarly to the traditional bridgeless structure presented in the previous paragraph, this architecture eliminates one diode in the current path and hence improves the efficiency.

Another interesting characteristic of this structure is that the PFC stage that is active, behaves as a conventional PFC boost would do:

- When the ”PH1” terminal is positive (see Figure 7a), diode D_1 opens and D_2 offers the return path. The input voltage for the ”PH1” PFC stage is a rectified sinusoid referenced to ground.
- For the other half−wave (see Figure 7b), when ”PH2” is the positive terminal, D_1 offers the return path. Diode D_2 is off and sees a rectified sinusoid that inputs the ”PH2” PFC stage. Again, we have a conventional PFC where the input voltage and the boost are traditionally referenced to ground.

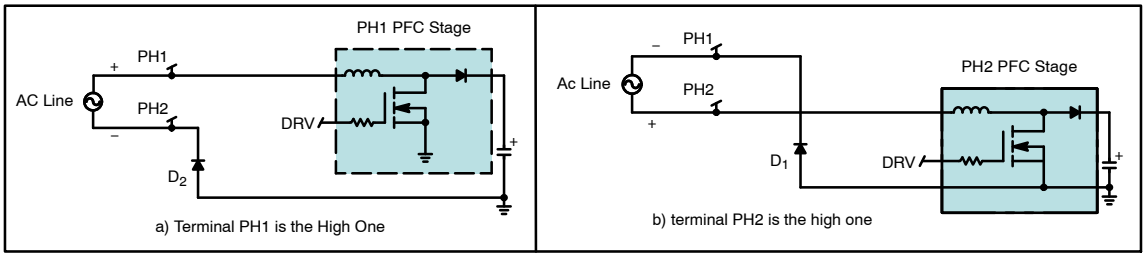

Figure 7. Equivalent Schematic for the Two Half−Waves

It is also worth noting that the 2−phase structure does not require any specific controller. The MOSFETs of the two branches are referenced to ground and they can be permanently driven even when their phase in idle phase. The MOSFET of the inactive branch would then be turned on and off useless but:

- At the benefit of a simplified circuitry since there is no need for detecting the active phase and for directing the drive signal to the right MOSFET according to the half−line cycle.
- At the price of the additional losses due to the inactive MOSFET drive. The loss is not very high anyway since the voltage across the MOSFET is null when its input voltage is zero. Hence, the gate charge to be provided is approximately halved compared to that of the active MOSFET.

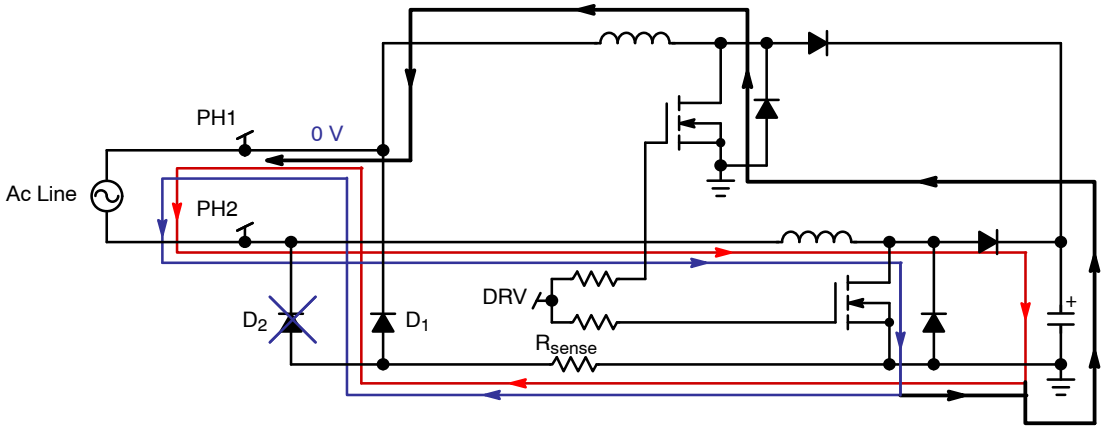

Figure 8. Operation for the ”PH2” Half−Wave

One should however note that the current does not necessary return by the D_1 and D_2 diodes. Figure 8 portrays the ”expected” current path when ”PH2” is high (the same analysis could have been done for ”PH1” high):

- The blue path is supposed to be the current path when the MOSFET is on
- The red one, that of the current when the MOSFET is open.

Actually, a large portion of the current flows as indicated in black.

This is because the body diode of the supposedly inactive MOSFET provides the current with another path. The coil exhibiting a low impedance at the line frequency, we have two diodes in parallel and the current share between them.

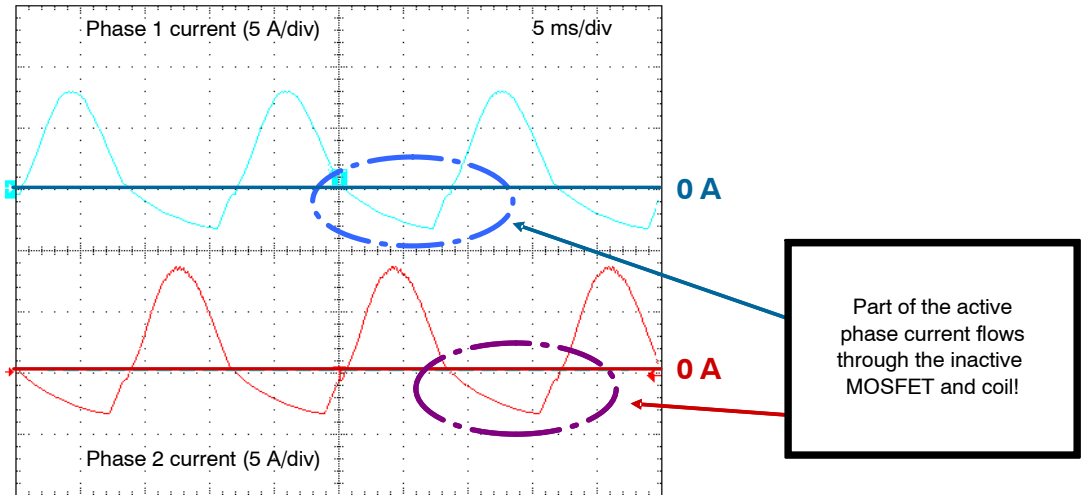

Figure 9. Part of the Current Flows through the Supposedly Inactive MOSFET and Coil

Figure 9 portrays the input current for each branch. One can see on this plot that a negative current takes place through the body diode during the ”inactive” half−wave. The main inconvenience of this behavior is that the input current cannot be sensed by inserting a R_{SENSE} resistor in the supposed return path (as shown by Figure 8) since part of current takes another road.

That is why current sense transformers can be of great help to measure the current in such a structure.

Implementation of the Bridgeless PFC

Figure 10 highlights the main parts of our 800 W prototype.

Diodes Bridge:

Amazingly, a diode bridge is implemented. However, it does not serve as a traditional input bridge to rectify the line (as shown by Figure 10, the two branches are directly connected to the line terminals). Here, the upper diodes (***D*****1** and ***D***3) simply derive the in−rush current that takes place when the PFC stage is plugged in (Note 2). Unless an overload situation occurs, these diodes are off for the rest of time.

The bottom diodes (***D*****2** and ***D***4) have the function that was described in the precedent section.

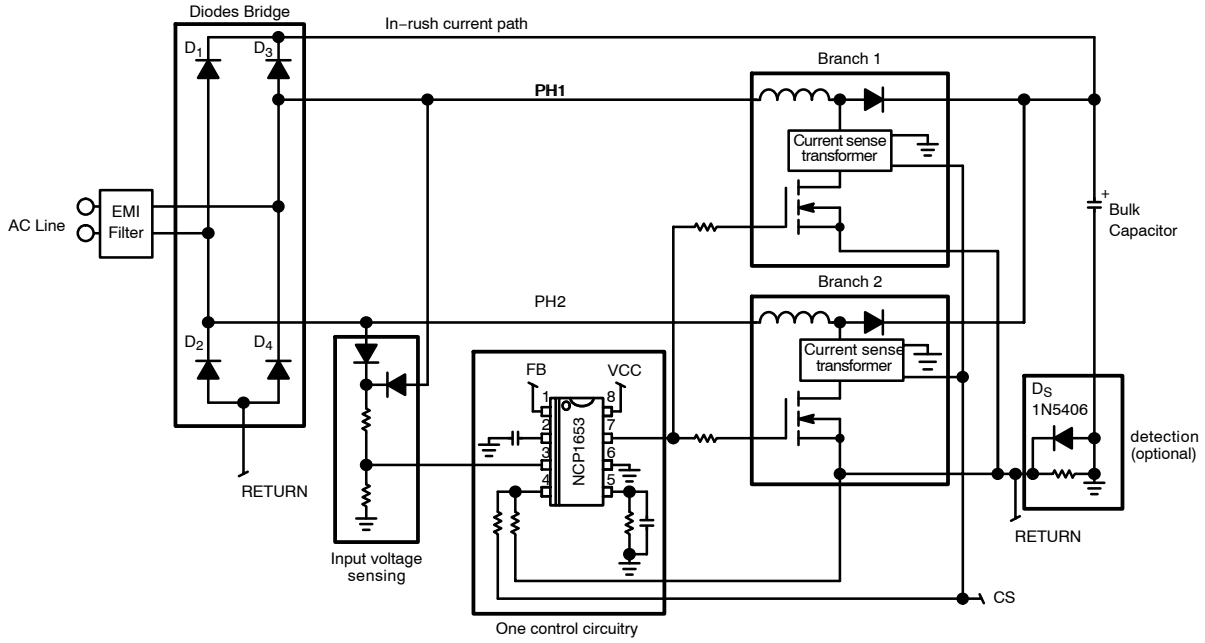

Figure 10. Simplified Application Schematic

2. As in a conventional PFC boost, there is no switch between the line and the bulk capacitor able to prevent the line from directly charge the bulk capacitor. That is why an in−rush takes place that charge the bulk capacitor to the line peak voltage. This in−rush current can be huge if not limited by some dedicated circuitry.

Input Voltage Sensing

The NCP1653 monitors the input voltage for feed−forward purpose. The NCP1654 further features a brown−out protection. As shown by Figure 10, two diodes are used that re−construct the rectified line voltage that can then be monitored by the circuit.

Branch 1 and Branch 2 PFC Boost:

Two PFC boost converters are to be designed. This application note does not focus on the dimensioning of the power components since it is relatively traditional. However, the fact that each branch is active for one half−line cycle only, improves the heating distribution. Also, the rms current being halved in each branch, the power components does not need to be as large as those of a conventional PFC.

Inrush Detection

Instead of a third current sense transformer, we made the choice to keep a current sense resistor to monitor the current that re−fuels the buck capacitor, i.e.:

- In−rush currents during the start−up phase or in over−load situations
- The current provided by the boost diodes in normal operation

Due to that, the MOSFET and the input bridge are referenced to the ”RETURN” potential instead of ground. The voltage between the RETURN and ground potentials is the negative voltage engendered by the R_{SENSE} resistor. If this voltage becomes too large (during in−rush sequences for instance), the MOSFETs' source potential may dramatically drop and some accidental MOSFET turn on may follow. That is why the voltage across the R_{SENSE} resistor is limited by a diode.

This diode must be able to sustain the in−rush current and its forward voltage must high enough so that the R_{SENSE} voltage is not clamped until the current largely exceeds its permissible level in normal operation. Otherwise, the clamping diode would prevent the R_{SENSE} voltage from becoming high enough to trigger the over−current protection.

Control Circuitry

As already mentioned, the 2−phase bridgeless PFC does not require any complex control circuitry. The NCP1653 PFC controller directly drives the two branches. The NCP1653 is a compact 8−pin PFC controller that operates in continuous conduction mode. As it directly adjusts the conduction time as a function of the coil current, there is no inner current loop to be compensated for an eased design. Housed in a DIP8 or SO8 package and available in two frequency versions (67 kHz or 100 kHz), the NCP1653 integrates all the features necessary for a compact and rugged PFC stage including a current sensing technique that allows the use of very low impedance, current sense resistors for reduced losses and a significant improvement of the efficiency. Compared to traditional solutions, the efficiency increase can be as high as almost 1%.

The NCP1654 is a NCP1653 derivative that further incorporates a brown−out detection block to disable the PFC stage when the line magnitude is too low. Also, the voltage regulation is made more accurate and a dynamic response enhancer dramatically minimizes the large deviation of the output voltage that a sharp line/load step could otherwise produce (see [4] and [5]).

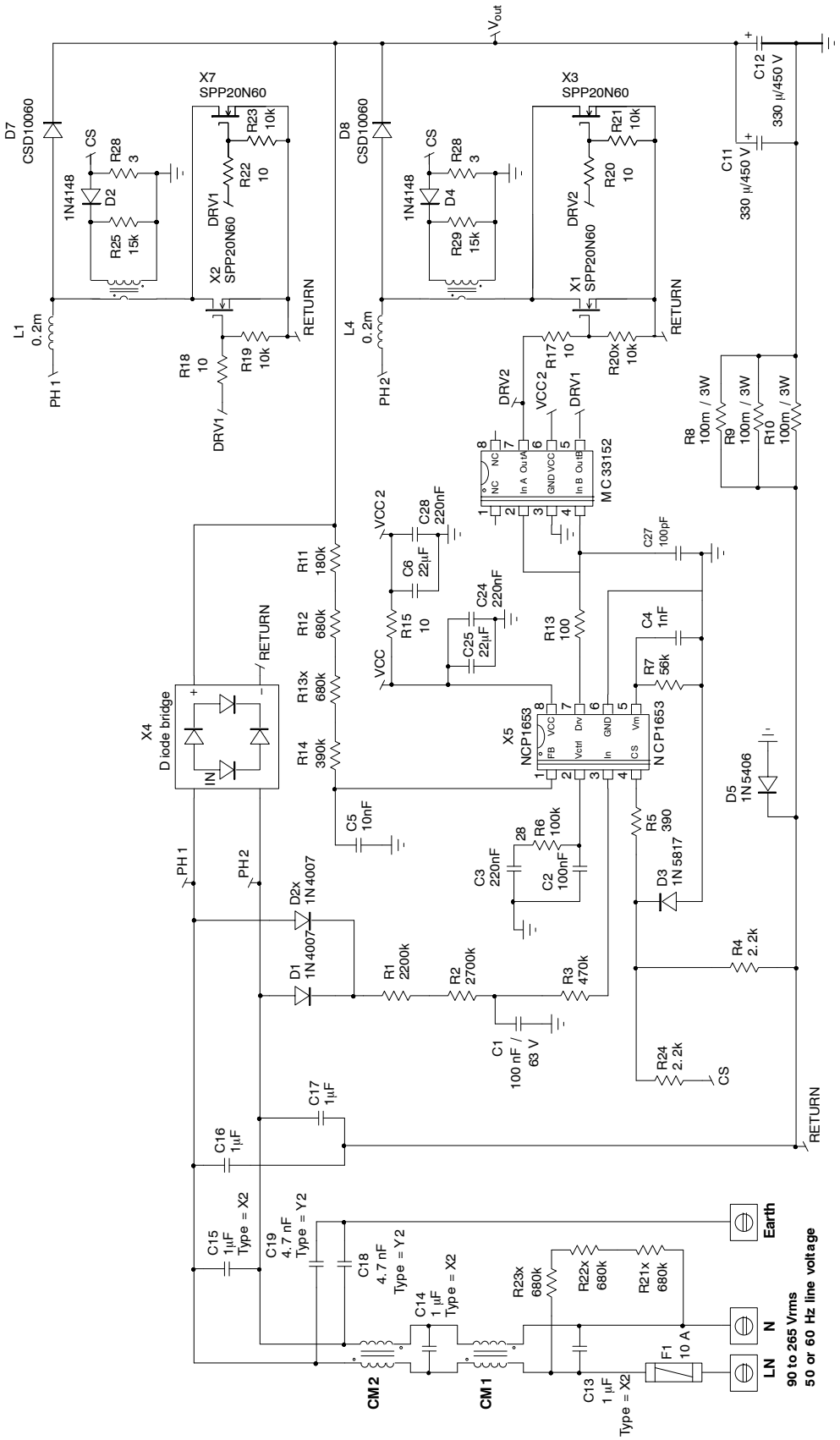

Figure 11. Application Schematic

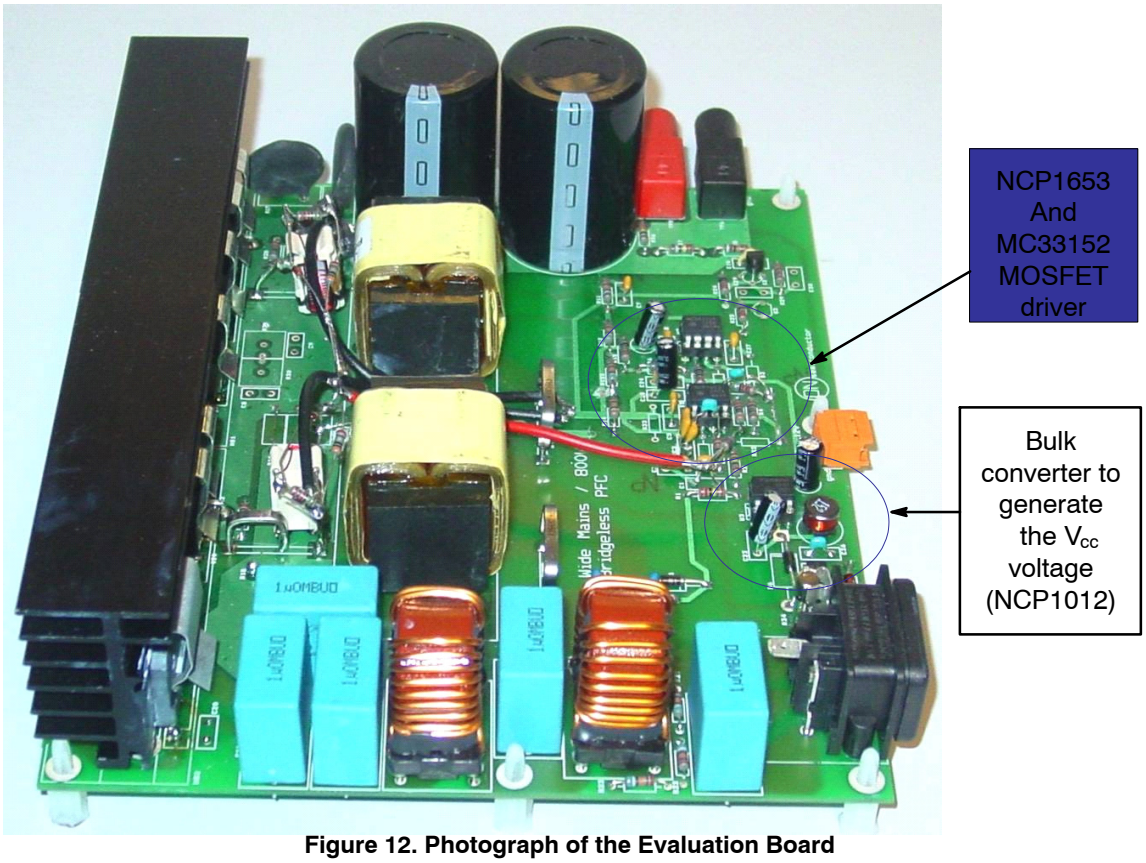

Figure 12. Photograph of the Evaluation Board

Main components of the board:

- Diodes Bridge (1 for the application): GSIB1580 from Vishay (15 A, 800 V)
- Current sense transformers (1 per branch): WCM601−2 from West Coast Magnetics (20 A, 50 turns)
- Boost diodes (1 per branch): CSD10060 (10 A, 600 V SiC diode from CREE)
- Power MOSFETs (2 per branch): SPP20N60 from Infineon (20 A, 600−V, 0.19 Ω)
- Inductors (1 per branch): 200 µH / 9.7 A_{rms} / 16 A_{pk} / 5 A_{pp} coil (ferrite core)
  Part Name: PFC−Choke LDU80025
  Part Number: 203860
  Producer: www.J−Lasslop.de, Information: Info@J−Lasslop.de
- Controller (only 1 for the application): NCP1653: 100 kHz, 8−pin, Continuous Conduction Mode PFC that can be easily replaced by its NCP1654 derivative that further features a brown−out protection and a dynamic response enhancer (see [4] and [5]).

Performance of the 800−W board

− Typical Waveforms

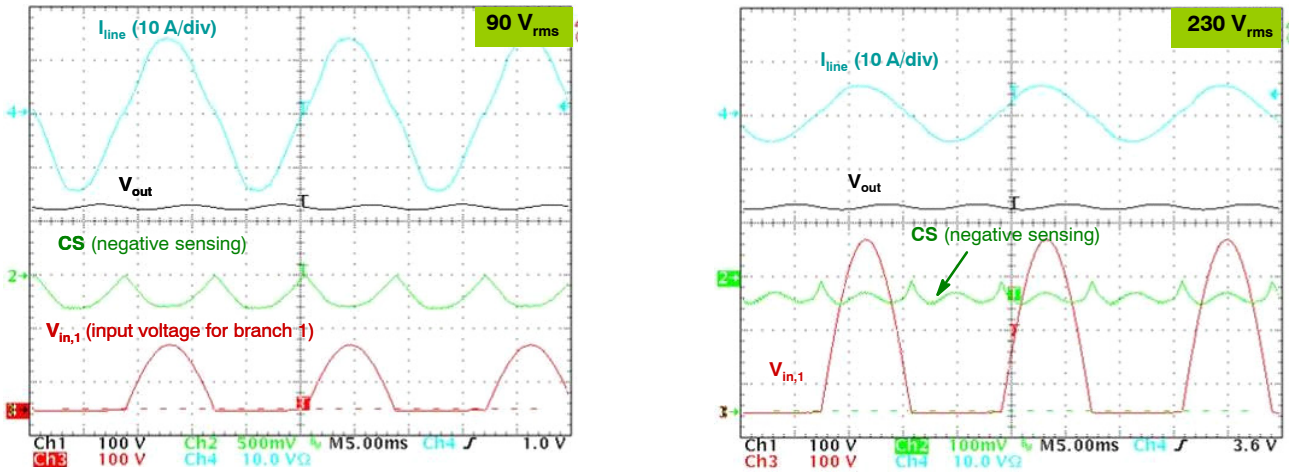

Figure 13. Typical Waveforms at Low Line (Left) and High Line (Right)

Plots Figure 13 of portray typical waveforms at full load (I_{out} = 2.1 A). ”CS” is the negative voltage provided by the current sense transformers. It is representative of the current flowing into the MOSFETs of the two branches (”CS” is the common output of the two current sense transformers). As expected, the input voltage of the ”PH1 PFC stage” (”$V_{in,1}$”) is a rectified sinusoid for one half−line cycle and null for the other one. The line current is properly shaped.

Figure 14 provides a magnified view at the top of the line sinusoid. The switching frequency is 100 kHz. The signal ”V_{sense}” (identical to ”CS”) is a negative representation of the MOSFET current. The current sense transformers are wired so that only the current drawn by the MOSFET drain is monitored (possible current flowing in the opposite direction cannot be sensed).

The waveforms are similar to those of a traditional CCM PFC.

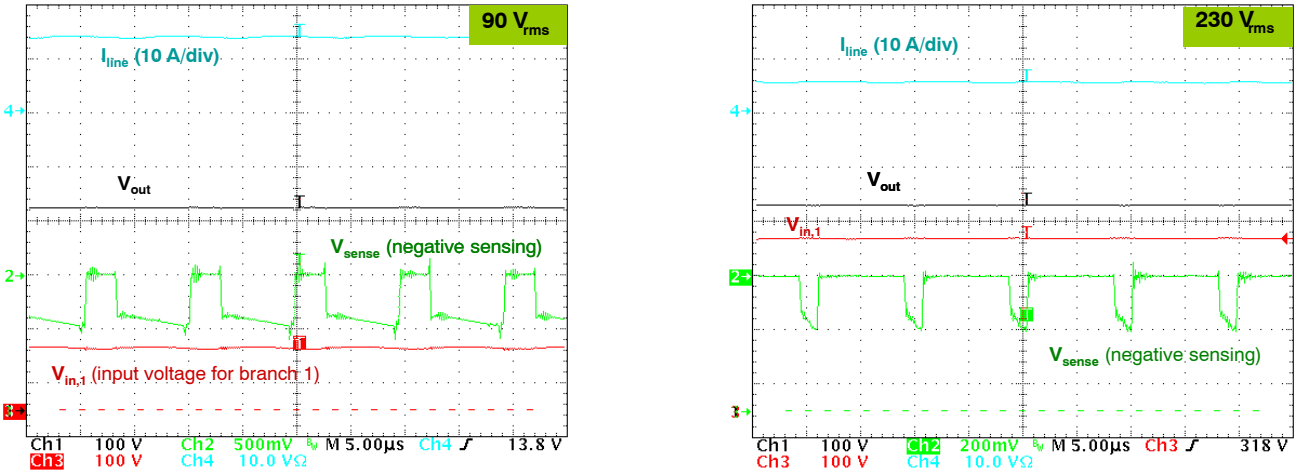

Figure 14. Magnified Views of Figure 13 Plots

Thermal Measurements

The following results were obtained using a thermal camera, after a 1/2 h operation. The board was operating at a 25°C ambient temperature, without fan. These data are indicative.

For the bridge, the MOSFETs and diodes, the measures were actually made on the heat−sink as near as possible of the components of interest.

Measurement Conditions:

$V_{in(rms)}$ = 88 V
$P_{in(avg))}$ = 814 W
V_{out} = 381 V
I_{out} = 2 A
PF = 0.995
THD = 9 %

Devices	Bridge	MOSFET1	Diode1	Coil1	MOSFET2	Diode2	Coil2	Bulk Capacitor	CM EMI coil
Temperature (°C)	85	95	77	47	86	80	48	40	45

Efficiency and Total Harmonic Distortion

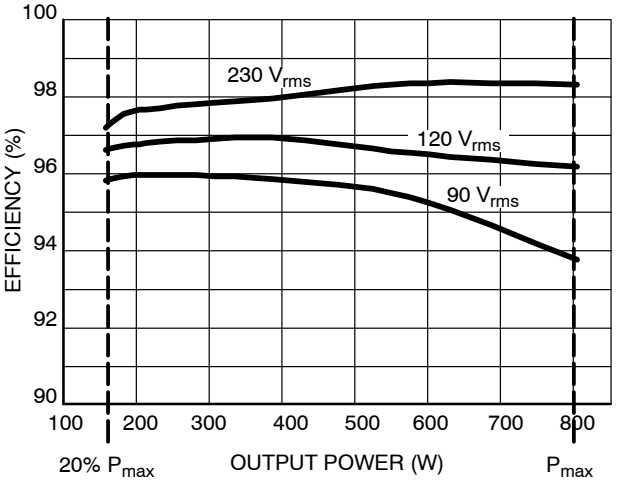

Figure 15. Efficiency Performance

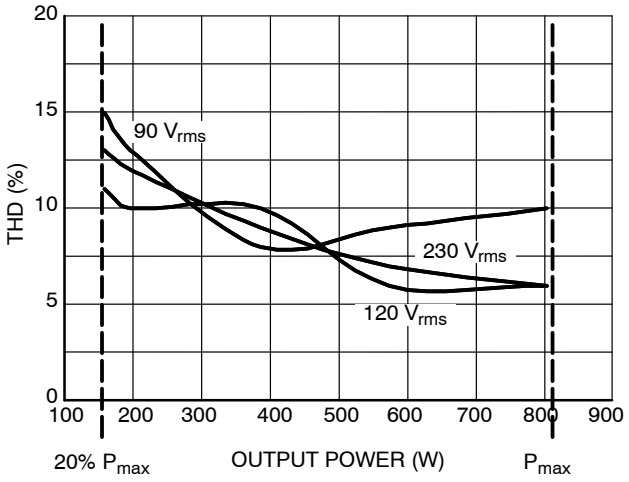

Figure 16. Total Harmonic Distortion Over the Load Range

Figure 15 portrays the efficiency over the line range, from 20% to 100% of the load.

The efficiency was measured in the following conditions:

- The measurements were made after the board was 30 mn operated full load, low line
- All the measurements were made consecutively without interruptions
- PF, THD, $I_{in(rms)}$ were measured by a power meter PM1200
- $V_{in(rms)}$ was measured directly at the input of the board by a HP 34401A multi−meter
- V_{out} was measured by a HP 34401A multi−meter
- The input power was computed according to:

$$P_{in(avg)} = V_{in(rms)} \cdot I_{in(rms)} \cdot PF$$

- Open Frame, Ambient Temperature, No Fan

To the light of Figure 15, we can note that:

- Like in a conventional PFC, the efficiency is higher at high line. In fact, this is because as in any boost, the losses are reduced when the ratio $\left(\frac{V_{in}(t)}{V_{out}}\right)$ is high (close to 1).
- At low line (90 V_{rms}), full load, the efficiency is in the range of 94% without a fan. It was even measured that @ 100 V_{rms}, we reach 95% at full load.
- We can note that the efficiency is high at light load. For instance, at 20% of full load, efficiency is in the range or higher than 96%.

Figure 16 portrays the THD at 90, 120 and 230 V_{rms} over the load. One can note that the total harmonic distortion remains very low even in high line, light load (< 15%) where the line current is small and more sensitive to all the sources of distortion like the system inaccuracies and mainly the EMI filter.

Conclusion

A bridgeless PFC based on the 2−phase architecture has several merits among which one can list the ease of control or the absence of high frequency noise injected to the line (eased EMI).

The paper presents the performance of a prototype controlled by the NCP1653 (100 kHz version). The NCP1654 that further incorporates the brown−out protection and a dynamic response enhancer could be implemented as well.

The prototype has been tested at full load (800 W output) without a fan (open frame, ambient temperature). In these conditions, the full−load efficiency was measured in the range of 94% at 90 V_{rms} and as high as 95% at 100 V_{rms}.

The THD remains very low.

A NCP1653 or NCP1654 driven 2−phase bridgeless PFC is a solution of choice for very efficient, high power applications.

References

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